2D Materials

PAPER

From bidirectional rectifier to polarity-controllable transistor in black phosphorus by dual gate modulation

To cite this article: Guocai Wang *et al* 2017 *2D Mater.* **4** 025056

View the article online for updates and enhancements.

Related content

- Semiconducting properties of bilayer graphene modulated by an electric field for next-generation atomic-film electronics
K Tsukagoshi, S-L Li, H Miyazaki et al.

- Toward high-performance two-dimensional black phosphorus electronic and optoelectronic devices
Xuefei Li, Xiong Xiong and Yanqing Wu

- WSe2/MoS2 and MoTe2/SnSe2 van der Waals heterostructure transistors with different band alignment
Chao Li, Xiao Yan, Xiongfei Song et al.

This content was downloaded from IP address 159.226.35.207 on 03/11/2017 at 17:04

IOP Publishing 2D Mater. 4 (2017) 025056 https://doi.org/10.1088/2053-1583/aa6535

2D Materials

RECEIVED
9 December 2016

REVISED
27 February 2017

ACCEPTED FOR PUBLICATION
7 March 2017

PUBLISHED
24 March 2017

PAPER

From bidirectional rectifier to polarity-controllable transistor in black phosphorus by dual gate modulation

Guocai Wang[1,2], Lihong Bao[1,2], Ruisong Ma[1,2], Tengfei Pei[1,2], Yu-Yang Zhang[1,3], Liangmei Wu[1,2], Zhang Zhou[1,2], Haifang Yang[1], Junjie Li[1], Changzhi Gu[1], Shixuan Du[1,2], Sokrates T Pantelides[1,3] and Hong-Jun Gao[1,2]

1 Institute of Physics &University of Chinese Academy of Sciences, Chinese Academy of Sciences, PO Box 603, Beijing 100190, People's Republic of China
2 Beijing Key Laboratory for Nanomaterials and Nanodevices, Beijing, 100190, People's Republic of China
3 Department of Physics and Astronomy, Vanderbilt University, Nashville, TN, 37235, United States of America

E-mail: lhbao@iphy.ac.cn

Keywords: black phosphorus, cross-linked PMMA, bidirectional rectifier, polarity-controllable transistor, dual gate modulation

Supplementary material for this article is available online

Abstract

In complementary metal oxide semiconductor (CMOS) technology, well-defined unipolar transport in field-effect transistors (FETs) is a basic requirement for logic operations, which can be realized by controllable doping of the semiconductor with electrons (n-type) or holes (p-type). However, recent demonstration of polarity controllable transistors in 2D semiconductors provides a flexible way in circuit design with increased circuit integration density. Here we demonstrate the conversion of a bidirectional rectifier to a polarity-controllable transistor in black phosphorus (BP) by dual gate modulation. Electrical characterization of the BP bidirectional rectifier reveals a current rectification of ~35 at room temperature that increases to ~350 upon lowering the temperature to 110 K. Employing cross-linked PMMA as a top gate and combining it together with the global back gate of the SiO_2 substrate, well-defined unipolar transport (n- or p-type) in BP could get accessed. This successful realization of polarity-controllable transistor in BP provides an alternative design for development of BP logic electronics.

Two-dimensional (2D) semiconductors have attracted significant attention in the past several years since the discovery of graphene [1–5]. However, the lack of a band gap in graphene and a combination of low charge-carrier mobility and large contact resistance in transition-metal dichalcogenides (TDMCs) as a result of Fermi level pinning have greatly constrained their applications in digital electronic devices [4, 6–9]. As a result, new layered 2D materials with a sizable band gap and high carrier mobility have been continuously investigated. One such material is black phosphorus (BP). BP is a p-type semiconducting nanomaterial with sizeable band gap from ~0.3 eV in bulk form to ~1.2 eV in monolayer form, hole mobilities of ~200–1000 cm^2 ($V^{-1} * s^{-1}$) at room temperature, and anisotropic transport characteristics [9–17]. Based on these superior properties, various BP devices, such as FET, phototransistors, heterojunctions, gas sensors, complementary logic inverters and so on, have been demonstrated since its discovery [10, 18–27].

Rectifiers, based on PN junctions and conventionally fabricated either by selectively chemically doping a bulk semiconductor to form a graded junction or by growing one type of semiconductor onto another type to form abrupt junction, are widely used rectifier circuits, detection circuit, voltage regulator circuits and modulation circuits [21]. Since the discovery of 2D materials such as graphene, TMDCs, and BP, various PN junctions based on them have been fabricated, featuring gate-tunable unipolar current rectification capability, photoelectric property, and much smaller device scale [18, 19, 21, 28–33]. Recently a new kind of three-terminal device called bidirectional rectifier was introduced, showing a unique bidirectional current-rectifying ability [34]. The BP bi-directional rectifier contains a back-gate tunable horizontal homojunction created by combining two gated BP diodes back-to-back in series. During its operation, the properties of BP and its high current rectification ability could be maintained.

© 2017 IOP Publishing Ltd

In order to use 2D semiconductor materials in complementary-metal-oxide-semiconductor (CMOS) circuits, control over the polarity, either p type or n type, is a basic requirement. Various methods, such as surface charge transfer, changing contact metal, local electrostatic gating, and using an electric double layer, have been developed to control the polarity of conduction in BP FETs [8, 29, 35–42]. Most of these methods yield BP FETs with fixed polarities (either n- or p-type) and cannot be tuned after their fabrication process. Recently, however, the concept of polarity-controlled transistor has been introduced, where the polarity of the transistor can be reversed by an electrical signal [43–45]. Achieving polarity-controllable transistors through electrical control may reduce the integration density of transistors compared to those with specific polarity (either electron- or hole-type) in the conventional semiconductor industry, but it provides an option for flexible design of logic circuits [4, 43, 44, 46]. Similar to ambipolar transistors, the key to realize the polarity-controlled FET through electrical modulation is the injection of electrons and holes to the transport channel through the same Schottky junction, where the carrier injection could be enhanced both by thermal emission and tunneling through a thinner the barrier [8, 38, 47, 48]. In BP bidirectional rectifiers, a potential barrier is introduced into the middle of the transport channel through charge-transfer doping of cross-linked PMMA and the barrier height could be tuned through a global back gate bias [34], suggesting such a device structure could be a potential candidate for polarity-controllable transistors.

In this work, we demonstrate the realization of polarity-controllable transistors in BP, from a bidirectional rectifier through a dual gate modulation. The BP bidirectional rectifier has been fabricated by placing a strip of cross-linked PMMA in the central part of an ordinary BP FET. Electrical characterization reveals its gate-tunable bidirectional rectifying capability with a rectification ratio of ~35, which increases to 3.5 * 10^2 when the temperature is lowered from 300 to 110 K. By employing the cross-linked PMMA as top gate, the on/off state of BP bidirectional rectifier can be controlled. When the width of the cross-linked PMMA strip is decreased, rectification capability of the BP bidirectional rectifier is disappeared and it works the same as an ordinary BP FET. By applying a positive top gate voltage bias $V_{tg} = 40$ V, the current rectification capability emerges again, indicating the conversion of BP FET into BP bidirectional rectifier by top gate modulation. Finally, by combining cross-linked PMMA top gate with the global back gate, the polarity of the BP transistor can be electrostatically reversed, realizing unipolar n-type or p-type conduction. The success of polarity-controllable BP transistors may contribute to the flexible design of logic circuits.

BP thin flakes (8–10 nm) were mechanically exfoliated using the Scotch tape method in a glove box environment and transferred onto a degenerately p-doped Si/SiO_2 (300 nm) substrate. The target BP flakes were then identified *in situ* by an optical microscope. To minimize the BP degradation, before taken out for device fabrication, the exfoliated flakes were immediately covered with a layer of PMMA (950, A5) which acts as a resist in the microfabrication process. Electron-beam lithography was employed to define the electrical contact, and a metal stack of Ni/Au (5/60 nm) was deposited by thermal evaporation. After lift-off in acetone, the Si/SiO_2 was quickly covered with a layer of PMMA (950, A5) at 4000 rpm for 60 s and baked at 180 °C. On the selected region of each BP flake, the PMMA was irradiated by 10 KV electrons at a dose of 15 000 μC cm^{-2}, forming the cross-linked PMMA strips that functions as dielectric for the top gate. The unexposed PMMA can be removed by soaking the chip in acetone for 10 min. Finally, a top gate electrode of Ni/Au (5/60 nm) was evaporated onto the cross-linked PMMA after a standard electron beam lithography process. Although the device fabrication process consists of many steps, the device features are well reproduced in most devices that are deemed identical (>80%). In the devices from the same batch (same exfoliation process), over 90% of devices show the same device features. Room temperature measurements on the devices are performed in a vacuum chamber with pressure lower than 10^{-5} Torr using a Keithley 4200-SCS system. The low-temperature measurements on the devices are performed in a home-designed four-probe scanning tunneling microscope with a cryostat using liquid N_2 or helium in continuous flow as cooling media.

A BP bidirectional rectifier is fabricated via selectively doping with cross-linked PMMA as the previous description [34]. A schematic diagram and optical image of it are shown in figures 1(a) and (b), respectively. Due to the doping effect of cross-linked PMMA, two obvious minima can be seen in the transfer curve of the device as shown in figure 1(c), which can be viewed as the superposition of the transfer curve of bare BP and the n-doped BP covered with cross-linked PMMA [49]. A potential barrier is inevitably formed between the bare BP and the PMMA-covered BP, which can be tuned by back gate modulation [34]. Figure 1(d) shows the linear plot of the output characteristics of this bi-directional rectifier at room temperature, and figure 1(e) is the corresponding logarithmic plot. When the back gate voltage is swept from −3 to 1 V, the current rectification ratio (defined as the ratio of saturation current at positive voltage bias to that of negative current bias) increases from ~10 to ~10^2. However, when V_{bg} is further increased to 3 V, a decrease of the rectification ratio is observed, indicating the tunability of the barrier height by back-gate voltage bias. Output characteristics of the device with $V_{bg} = 0$ V at temperature from $T = 110$ K to $T = 300$ K is shown in figure 1(f). The current rectification reaches its maximum of ~3.5 * 10^2 at $T = 110$ K, and decreases to ~35 at room temperature with temperature increasing, due to the fact that at low temperatures much fewer charge

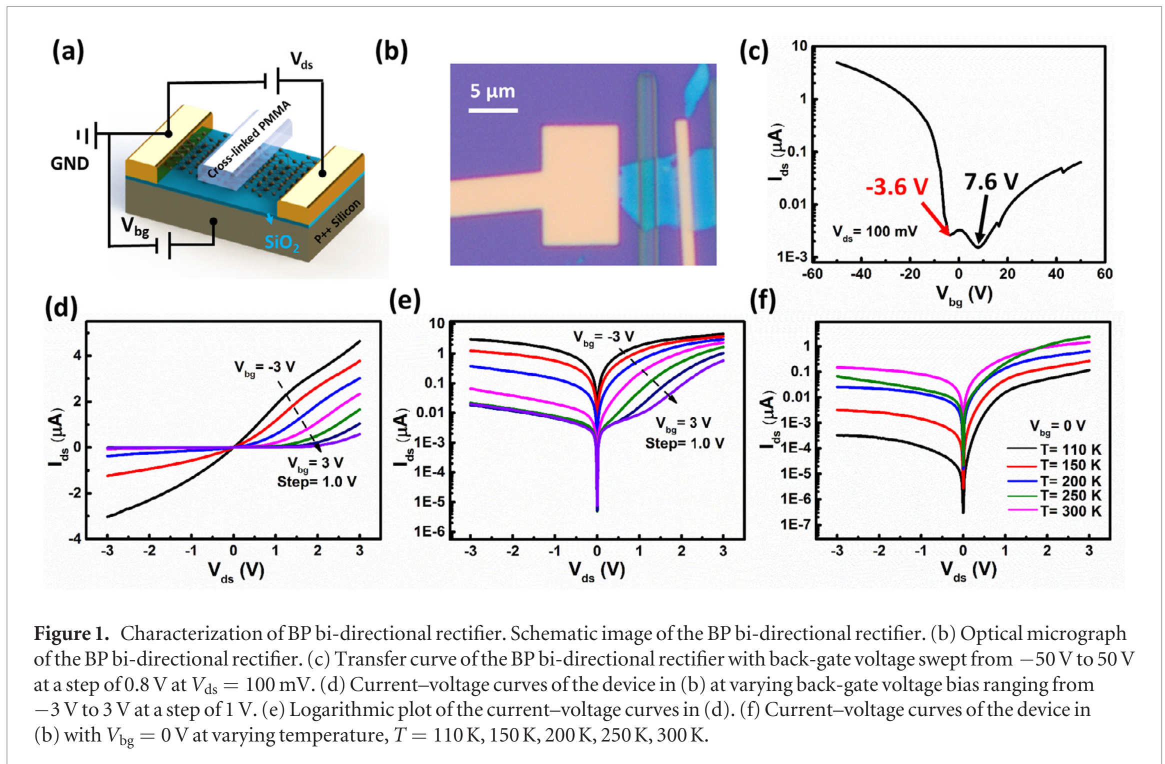

Figure 1. Characterization of BP bi-directional rectifier. Schematic image of the BP bi-directional rectifier. (b) Optical micrograph of the BP bi-directional rectifier. (c) Transfer curve of the BP bi-directional rectifier with back-gate voltage swept from −50 V to 50 V at a step of 0.8 V at V_{ds} = 100 mV. (d) Current–voltage curves of the device in (b) at varying back-gate voltage bias ranging from −3 V to 3 V at a step of 1 V. (e) Logarithmic plot of the current–voltage curves in (d). (f) Current–voltage curves of the device in (b) with V_{bg} = 0 V at varying temperature, T = 110 K, 150 K, 200 K, 250 K, 300 K.

carriers can gain enough energy to overcome the barrier within the channel.

In practical applications, a well-defined unipolar transport in FETs is essential for logical operation. To get access to the unipolar transport in BP, a BP FET with both top gate and back gate modulation is fabricated, in which cross-linked PMMA is employed as top gate dielectric, as schematically shown in figure 2(a). Although a narrower cross-linked PMMA strip is fabricated compared to that of figure 1(b), the transfer curve still shows two typical current minima as shown in figure 2(c). This is the result of the initial doping effect of the cross-linked PMMA dielectric. When a top gate voltage $V_{tg} = -20$ V is applied, the current minimum in the transfer curve on the hole conduction side ($V_{bg} > 0$) disappears, while the one on the electron conduction side ($V_{bg} < 0$) is shifted toward the electron doping side, indicating the suppression of electron doping in BP by depletion of interfacial charges between cross-linked PMMA and BP. The output characteristics of the device at top gate voltage bias of 0 (blue) and −20 V (black) is shown in figure 2(d), respectively. The current rectification behavior almost disappears when $V_{tg} = -20$ V, demonstrating that the top gate voltage can be utilized to control the on/off state of the bidirectional rectifier. Moreover, when the width of the cross-linked PMMA strip is decreased, as shown in figure 3(a), the transfer curve at zero top-gate voltage bias shows p-type dominated ambipolar behavior like a pure BP FET. This is attributed to the smaller interfacial charges introduced to the interface between the BP flake and cross-linked PMMA and cannot effectively shift the threshold voltage to the electron conduction side. An optical micrograph of this device is shown in the inset. When a positive top gate voltage $V_{tg} = 40$ V is applied, the current minimum on the electron doping side ($V_{bg} < 0$) appears again, showing that by applying a positive top gate voltage, a BP bidirectional rectifier can be realized in an ordinary BP FET, as shown in figure 3(b). The output curve of the device under different top gate voltage bias is shown in figure 3(c), indicating different current rectifying behavior. The output characteristics shown in figure 3(d) reveal that, at the specific top gate voltage $V_{tg} = 40$ V, the rectification behavior of the device can be tuned by the back voltage sweeping from −6 to +6 V.

Moreover, by combining the global back gate and the local top gate together, electrostatically reversible polarity transport in BP can be obtained. Figure 4(a) is a color contour showing how the current through the channel changes with both the top gate and the back gate voltage biases, which clearly reveals that through top and back gate voltage modulation, unipolar transport in BP can be realized. The current reaches its extreme values with the condition of $V_{tg} < 0$, $V_{bg} < 0$, and $V_{tg} > 0$, $V_{bg} > 0$, respectively, in which the top and back gate bias induce the same type of charge carriers labeled as P/P/P and N/N/N. However, with $V_{tg} < 0$ and $V_{bg} > 0$ bias condition, the carriers in the channel can be labelled as N/P/N, and with $V_{tg} > 0$, $V_{bg} < 0$, the carriers can be identified as P/N/P (light blue region in figure 4(a)), where the current minimum can be observed. The current minimum has two origins: (1) The top gate voltage bias induces depletion of the charge carriers in the channel, i.e. the carrier density within the channel is decreased; (2) A junction is formed at the interface between the BP underneath the top gate and the pure part, which will prevent the charge carriers flowing from the source to the drain. As a result, the channel resistance increases. Figures 4(b)

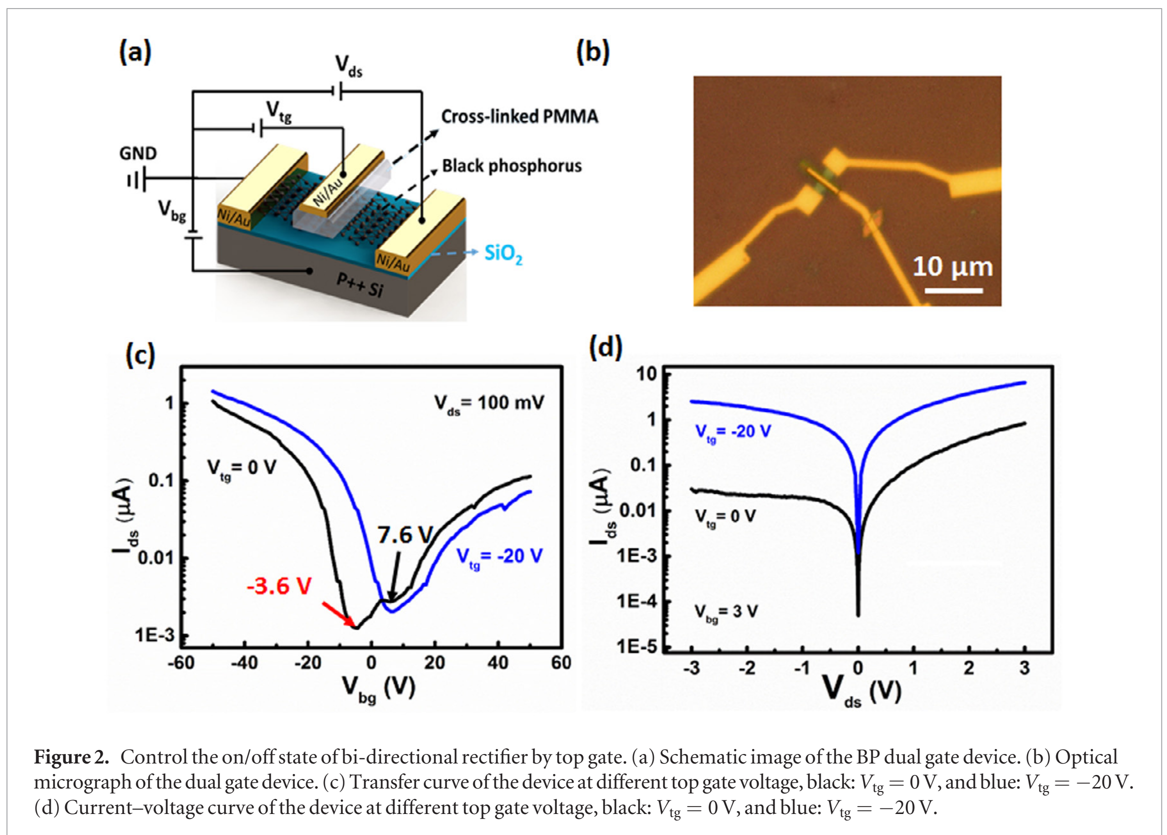

Figure 2. Control the on/off state of bi-directional rectifier by top gate. (a) Schematic image of the BP dual gate device. (b) Optical micrograph of the dual gate device. (c) Transfer curve of the device at different top gate voltage, black: $V_{tg} = 0$ V, and blue: $V_{tg} = -20$ V. (d) Current–voltage curve of the device at different top gate voltage, black: $V_{tg} = 0$ V, and blue: $V_{tg} = -20$ V.

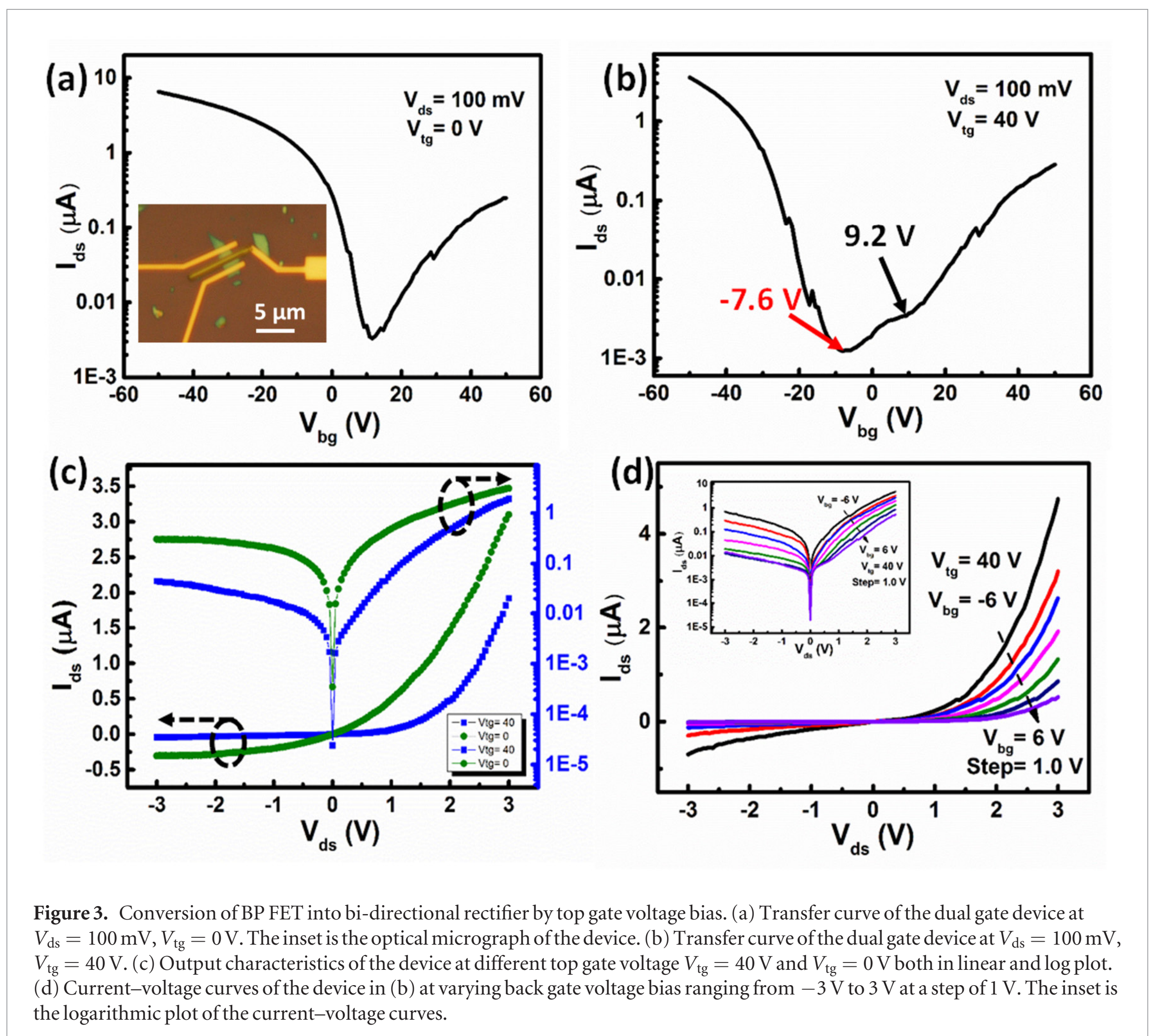

Figure 3. Conversion of BP FET into bi-directional rectifier by top gate voltage bias. (a) Transfer curve of the dual gate device at $V_{ds} = 100$ mV, $V_{tg} = 0$ V. The inset is the optical micrograph of the device. (b) Transfer curve of the dual gate device at $V_{ds} = 100$ mV, $V_{tg} = 40$ V. (c) Output characteristics of the device at different top gate voltage $V_{tg} = 40$ V and $V_{tg} = 0$ V both in linear and log plot. (d) Current–voltage curves of the device in (b) at varying back gate voltage bias ranging from -3 V to 3 V at a step of 1 V. The inset is the logarithmic plot of the current–voltage curves.

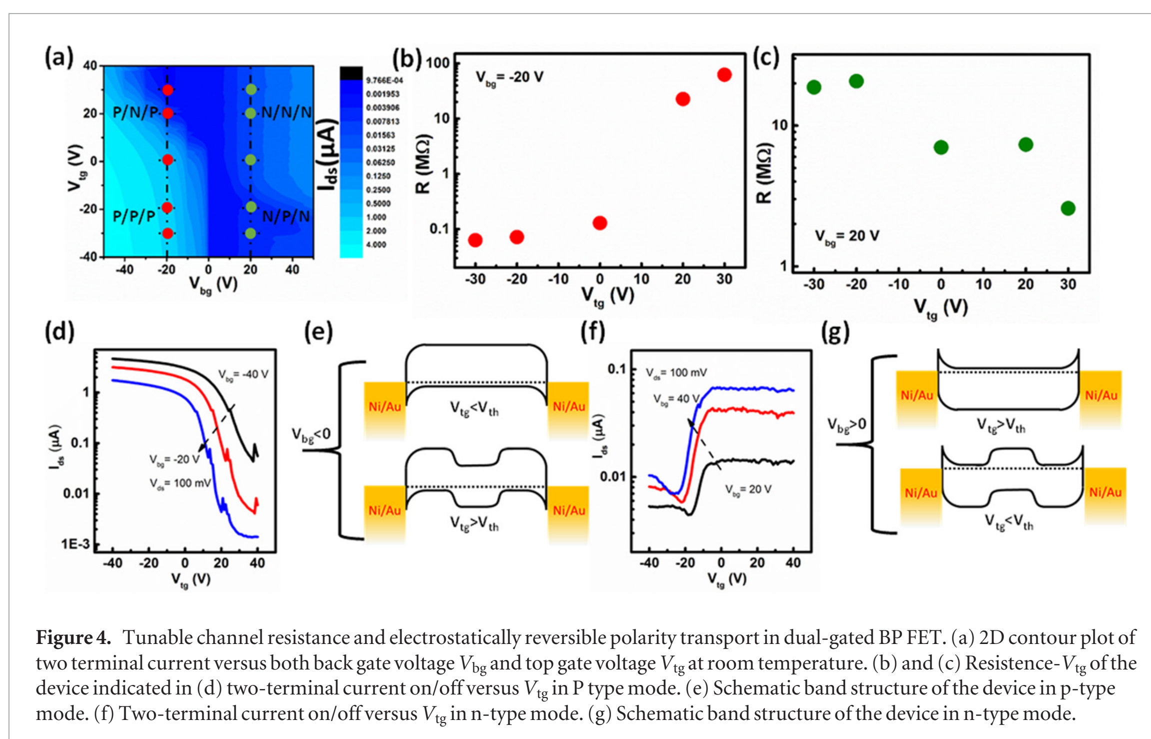

Figure 4. Tunable channel resistance and electrostatically reversible polarity transport in dual-gated BP FET. (a) 2D contour plot of two terminal current versus both back gate voltage V_{bg} and top gate voltage V_{tg} at room temperature. (b) and (c) Resistence-V_{tg} of the device indicated in (d) two-terminal current on/off versus V_{tg} in P type mode. (e) Schematic band structure of the device in p-type mode. (f) Two-terminal current on/off versus V_{tg} in n-type mode. (g) Schematic band structure of the device in n-type mode.

and (c) show how the resistance changes with the dual gate modulation (V_{bg} = 20 or −20 V, while V_{tg} varies from −30 to 30 V), indicated by red and green circles in figure 4(a), respectively. From figure 4(b) we can see that the resistance of the channel increases with the top gate voltage bias and can be varied by three orders of magnitude when the top gate is biased from $V_{tg} = -30$ V to $V_{tg} = 30$ V at constant back-gate voltage bias $V_{bg} = -20$ V. Apparently, unipolar p-type transport can be achieved when the back gate is negatively biased and sweeping the top gate from −30 to 30 V, as shown in the transfer curve of figure 4(d). A schematic of the energy band diagram is shown in figure 4(e). Similarly, when the back gate voltage is positively biased, by varying the top gate voltage from −30 to 30 V, unipolar n-type transport can also be achieved, as shown in the transfer curve of figure 4(f). Figure 4(g) shows the energy band diagram under these bias conditions. Therefore, through dual-gate modulation, both n-type and p-type unipolar transport in BP can be obtained.

In summary, polarity-controllable transistor in BP has been successfully realized by electrical reversal of a BP bidirectional rectifier via dual gate modulation, where cross-linked PMMA is employed as a top gate dielectric. This device configuration is expected to be applicable to other 2D semiconductors and may contribute to the flexible design of electronics in the future.

Acknowledgments

This work is supported by National '973' Projects of China (Grants No. 2013CBA01600), National Key Research & Development Projects of China (Grants No. 2016YFA0202300), National Natural Science Foundation of China (Grants No. 61474141, 61674170, 61335006, 61390501, 51325204, 51210003), the Chinese Academy of Sciences (CAS), and Youth Innovation Promotion Association of CAS (20150005). STP's work at ORNL was supported by US DOE Office of Basic Energy Sciences (Grant No. DE-FG02-09ER46554) and by the McMinn Endowment at Vanderbilt. YYZ and STP acknowledge National Center for Supercomputing Applications which is supported by the DOE Office of Science under Contract No. DE-AC02-05CH11231, and the Extreme Science and Engineering Discovery Environment (XSEDE) which is supported by National Science Foundation Grant No. ACI-1053575.

References

[1] Novoselov K S, Jiang D, Schedin F, Booth T J, Khotkevich V V, Morozov S V and Geim A K 2005 *Proc. Natl Acad. Sci. USA* **102** 10451–3
[2] Geim A K and Novoselov K S 2007 *Nat. Mater.* **6** 183–91
[3] Yazyev O V and Chen Y P 2014 *Nat. Nanotechnol.* **9** 755–67
[4] Fiori G, Bonaccorso F, Iannaccone G, Palacios T, Neumaier D, Seabaugh A, Banerjee S K and Colombo L 2014 *Nat. Nanotechnol.* **9** 768–79
[5] Koppens F H, Mueller T, Avouris P, Ferrari A C, Vitiello M S and Polini M 2014 *Nat. Nanotechnol.* **9** 780–93
[6] Schwierz F 2010 *Nat. Nanotechnol.* **5** 487–96
[7] Radisavljevic B, Radenovic A, Brivio J, Giacometti V and Kis A 2011 *Nat. Nanotechnol.* **6** 147–50
[8] Das S, Chen H Y, Penumatcha A V and Appenzeller J 2013 *Nano Lett.* **13** 100–5
[9] Liu H, Neal A T, Zhu Z, Luo Z, Xu X, Tomanek D and Ye P D 2014 *ACS Nano* **8** 4033–41
[10] Li L, Yu Y, Ye G J, Ge Q, Ou X, Wu H, Feng D, Chen X H and Zhang Y 2014 *Nat. Nanotechnol.* **9** 372–7
[11] Liu H, Du Y, Deng Y and Ye P D 2015 *Chem. Soc. Rev.* **44** 2732–43
[12] Low T, Rodin A S, Carvalho A, Jiang Y, Wang H, Xia F and Castro Neto A H 2014 *Phys. Rev.* B **90** 075434
[13] Koenig S P, Doganov R A, Schmidt H, Castro Neto A H and Özyilmaz B 2014 *Appl. Phys. Lett.* **104** 103106
[14] Asahina H and Morita A 1984 *J. Phys. C: Solid State Phys.* **17** 1839–52

[15] Na J, Lee Y T, Lim J A, Hwang Do K, Kim G T, Choi W K and Song Y W 2014 *ACS Nano* **8** 11753–62
[16] Castellanos-Gomez A *et al* 2014 *2D Mater.* **1** 025001
[17] Du Y C, Liu H, Deng Y X and Ye P D 2014 *ACS Nano* **8** 10035–42
[18] Buscema M, Groenendijk D J, Steele G A, Van Der Zant H S and Castellanos-Gomez A 2014 *Nat. Commun.* **5** 4651
[19] Chen P *et al* 2015 *2D Mater.* **2** 034009
[20] Abbas A N, Liu B, Chen L, Ma Y, Cong S, Aroonyadet N, Kopf M, Nilges T and Zhou C 2015 *ACS Nano* **9** 5618–24
[21] Deng Y, Luo Z, Conrad N J, Liu H, Gong Y, Najmaei S, Ajayan P M, Lou J, Xu X and Ye P D 2014 *ACS Nano* **8** 8292–9
[22] Wang H, Wang X, Xia F, Wang L, Jiang H, Xia Q, Chin M L, Dubey M and Han S J 2014 *Nano Lett.* **14** 6424–9
[23] Su Y, Kshirsagar C U, Robbins M C, Haratipour N and Koester S J 2016 *2D Mater* **3** 011006
[24] Zhu W, Yogeesh M N, Yang S, Aldave S H, Kim J S, Sonde S, Tao L, Lu N and Akinwande D 2015 *Nano Lett.* **15** 1883–90
[25] Kim J S, Jeon P J, Lee J, Choi K, Lee H S, Cho Y, Lee Y T, Hwang Do K and Im S 2015 *Nano Lett.* **15** 5778–83
[26] Feng Z *et al* 2016 *2D Mater.* **3** 035021
[27] Castellanos-Gomez A 2015 *J. Phys. Chem. Lett.* **6** 4280–91
[28] Buscema M, Island J O, Groenendijk D J, Blanter S I, Steele G A, Van Der Zant H S and Castellanos-Gomez A 2015 *Chem. Soc. Rev.* **44** 3691–718
[29] Chen M, Nam H, Wi S, Ji L, Ren X, Bian L, Lu S and Liang X 2013 *Appl. Phys. Lett.* **103** 142110
[30] Choi J H, Lee G H, Park S, Jeong D, Lee J O, Sim H S, Doh Y J and Lee H J 2013 *Nat. Commun.* **4** 2525
[31] Oh G, Kim J S, Jeon J H, Won E, Son J W, Lee D H, Kim C K, Jang J, Lee T and Park B H 2015 *ACS Nano* **9** 7515–22
[32] Yu L, Zubair A, Santos E J, Zhang X, Lin Y, Zhang Y and Palacios T 2015 *Nano Lett.* **15** 4928–34
[33] Yang H, Heo J, Park S, Song H J, Seo D H, Byun K E, Kim P, Yoo I, Chung H J and Kim K 2012 *Science* **336** 1140–3
[34] Wang G *et al* 2016 *Nano Lett.* **16** 6870–8
[35] Koenig S P, Doganov R A, Seixas L, Carvalho A, Tan J Y, Watanabe K, Taniguchi T, Yakovlev N, Castro Neto A H and Ozyilmaz B 2016 *Nano Lett.* **16** 2145–51
[36] Liu H and Ye P D D 2012 *IEEE Electron Device Lett.* **33** 546–8
[37] Xiang D *et al* 2015 *Nat Commun.* **6** 6485
[38] Perello D J, Chae S H, Song S and Lee Y H 2015 *Nat. Commun.* **6** 7809
[39] Lohmann T, Von Klitzing K and Smet J H 2009 *Nano Lett.* **9** 1973–9
[40] Wang F, Stepanov P, Gray M, Lau C N, Itkis M E and Haddon R C 2015 *Nano Lett.* **15** 5284–8
[41] Khim D, Baeg K-J, Caironi M, Liu C, Xu Y, Kim D-Y and Noh Y-Y 2014 *Adv. Funct. Mater.* **24** 6252–61
[42] Zhang Y J, Ye J T, Yomogida Y, Takenobu T and Iwasa Y 2013 *Nano Lett.* **13** 3023–8
[43] Nakaharai S, Yamamoto M, Ueno K, Lin Y F, Li S L and Tsukagoshi K 2015 *ACS Nano* **9** 5976–83
[44] Lin Y M, Appenzeller J, Knoch J and Avouris P 2005 *IEEE Trans. Nanotechnol.* **4** 481–9
[45] De Marchi M, Zhang J, Frache S, Sacchetto D, Gaillardon P E, Leblebici Y and De Micheli G 2014 *IEEE Electron Device Lett.* **35** 880–2
[46] Nakaharai S, Iijima T, Ogawa S, Li S-L, Tsukagoshi K, Sato S and Yokoyama N 2014 *IEEE Trans. Nanotechnol.* **13** 1039–43
[47] Miyazaki H, Li S L, Nakaharai S and Tsukagoshi K 2012 *Appl. Phys. Lett.* **100** 2054–8
[48] Li H M, Lee D Y, Choi M S, Qu D, Liu X, Ra C H and Yoo W J 2014 *Sci. Rep.* **4** 4041
[49] Jariwala D 2013 *Proc. Natl Acad. Sci. USA* **110** 18076–80